

Electromagnetic Compatibility–Driven Design and Real-Time Control of Multilevel Inverters for Conducted EMI Reduction

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التصميم القائم على التوافق الكهرومغناطيسي والتحكم الآني في العواكس متعددة المستويات للحد من التداخل الكهرومغناطيسي الموصل

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Abstract

Multilevel inverters (MLIs), as a robust solution, have gained popularity for medium and high-power applications owing to its excellent quality of output waveforms, higher efficiency performance, lower switching stress and superior scalability over conventional two-level converters. The increasing use of these types of circuits by the implementation in renewable power systems, electric vehicles, smart grids, industrial motor drives and energy storage systems means electromagnetic compatibility (EMC) has become a significant issue for the design of most power electronics nowadays. Multilevel inverters are using high frequency causes to radiate EMI, but also the switching operation at multi-level inverter creates a major conducted EMI sources due to rapid voltage transitions, parasitic coupling effects and common-mode voltage generation. These disturbances can impair system reliability, reduce communication and sensing performance, and make compliance with international EMC standards more difficult.

Traditional EMI mitigation methods are largely based on passive filters or shielding structures, requiring modifications with changes to the grounding and direct re-design of hardware that add cost, size, weight and power losses in addition to leading to an after-the-fact manner of addressing EMI once converters have been developed. The above-mentioned methods are losing significance in modern power electronic systems which have higher switching frequencies, lower inductances and wide-bandgap semiconductors utilized. Therefore, this has led to the need for design approaches where EMC is integrated into inverter compensation and operation as part of control methodology rather than post-design compliance.

This paper presents an Electromagnetic Compatibility–Driven Design and Real-Time Control Framework for multilevel inverters to minimize conducted EMI at the source while preserving high-performance converter operation. The proposed methodology is a combination of inverter modelling, modulation strategy selection, switching-state control and real-time implementation in order to incorporate EMC requirements. To support controller design and performance analysis, a detailed inverter model including switching dynamics, parasitic components, common-mode behavior and conducted EMI propagation mechanisms is developed. Advanced EMC-aware control methods are used for conducted emission suppression, common-mode voltage and current reduction, power quality increase, and compliance with international EMC regulations.

To assess practicality under realistic operating conditions, the proposed framework has been implemented on real-time control platforms such as Digital Signal Processors (DSPs) and Field Programmable Gate

Arrays(FPGAs). The EMI measurements involve harmonic analysis, efficiency evaluation, common-mode behavior characterization and comparison against CISPR and IEC standards. The results show that, by integrating EMC considerations directly into controller design, it is possible to achieve significant source level EMI reduction without performance loss in the dynamic and power quality domain. The framework proposed in this study offers a practical and scalable approach to the development of next-generation EMC-compliant multilevel inverter systems for industrial, transportation, and renewable power generation applications.

Keywords: Electromagnetic Compatibility (EMC), Conducted Electromagnetic Interference (EMI), Multilevel Inverters, Real-Time Control, EMC-Driven Design, Digital Signal Processor (DSP), Field Programmable Gate Array (FPGA), Common-Mode Voltage, Common-Mode Current, Power Electronics, Renewable Energy Systems, Industrial Drives.

المخلص

تُعد العواكس متعددة المستويات (Multilevel Inverters - MLI) من الحلول المتقدمة والفعّالة في تطبيقات القدرة المتوسطة والعالية، وذلك بفضل قدرتها على إنتاج أشكال موجية عالية الجودة، وتحقيق كفاءة تحويل مرتفعة، وتقليل إجهاد عناصر التبديل، بالإضافة إلى قابليتها العالية للتوسع مقارنةً بالعواكس التقليدية ثنائية المستوى. ومع التوسع المتزايد في استخدام هذه العواكس في أنظمة الطاقة المتجددة، والمركبات الكهربائية، والشبكات الذكية، وأنظمة قيادة المحركات الصناعية، وأنظمة تخزين الطاقة، أصبح التوافق الكهرومغناطيسي (Electromagnetic Compatibility - EMC) أحد أهم التحديات التي تواجه تصميم وتشغيل أنظمة إلكترونيات القدرة الحديثة.

وعلى الرغم من المزايا العديدة للعواكس متعددة المستويات، فإن عمليات التبديل عالية التردد، والانتقالات السريعة للجهد، وتأثيرات الاقتران الطفيلي، وتوليد الجهد المشترك (Common-Mode Voltage) تؤدي إلى نشوء مستويات مرتفعة من التداخل الكهرومغناطيسي الموصل (Conducted Electromagnetic Interference - EMI). ويمكن لهذه الاضطرابات أن تؤثر سلبيًا على موثوقية النظام، وتقلل من كفاءة أنظمة الاتصالات والاستشعار، كما قد تعيق الامتثال للمعايير الدولية الخاصة بالتوافق الكهرومغناطيسي.

تعتمد معظم أساليب الحد من التداخل الكهرومغناطيسي التقليدية على استخدام المرشحات السلبية (Passive Filters)، أو أنظمة التدرج الكهرومغناطيسي (Shielding)، أو تحسينات التأسيس، أو إعادة تصميم العنود الإلكتروني. وعلى الرغم من فعالية هذه الحلول في تقليل الانبعاثات الكهرومغناطيسية، فإنها تؤدي غالبًا إلى زيادة حجم النظام ووزنه وتكلفته، بالإضافة إلى زيادة الفوائد الكهربائية. كما أنها تعالج مشكلة التداخل الكهرومغناطيسي بعد اكتمال تصميم المحول، بدلاً من دمج متطلبات التوافق الكهرومغناطيسي ضمن عملية التصميم نفسها. ومع الاتجاه المتزايد نحو استخدام ترددات تبديل أعلى، وتقنيات إلكترونيات القدرة المعتمدة على أشباه الموصلات واسعة النطاق (Wide-Bandgap Semiconductors)، أصبحت هذه الأساليب التقليدية أقل كفاءة وملاءمة للتطبيقات الحديثة.

يقدم هذا البحث إطارًا متكاملًا للتصميم القائم على التوافق الكهرومغناطيسي والتحكم الآني في العواكس متعددة المستويات بهدف تقليل التداخل الكهرومغناطيسي الموصل عند مصدره مع الحفاظ على الأداء العالي للمحول. تعتمد المنهجية المقترحة على دمج متطلبات التوافق الكهرومغناطيسي ضمن مراحل نمذجة العاكس، واختيار استراتيجيات التضمين، والتحكم في حالات التبديل، والتنفيذ الآني لخوارزميات التحكم.

ولتحقيق ذلك، تم تطوير نموذج تفصيلي للعاكس يأخذ في الاعتبار ديناميكيات التبديل، والعناصر الطفيلية، وسلوك الجهد المشترك، وآليات انتشار التداخل الكهرومغناطيسي الموصل. كما تم توظيف استراتيجيات تحكم متقدمة تراعي متطلبات التوافق الكهرومغناطيسي بهدف تقليل الانبعاثات الموصلة، وخفض الجهد والتيار المشتركين، وتحسين جودة القدرة الكهربائية، وضمان الامتثال للمعايير الدولية الخاصة بالتوافق الكهرومغناطيسي.

ولتقييم الجدوى العملية للإطار المقترح في ظروف التشغيل الواقعية، تم تنفيذ النظام على منصات تحكم آنية تشمل معالجات الإشارة الرقمية (Digital Signal Processors - DSPs) والمصفوفات المنطقية القابلة للبرمجة ميدانيًا (Field Programmable Gate Arrays - FPGAs). وقد شمل تقييم الأداء إجراء قياسات للتداخل الكهرومغناطيسي الموصل، وتحليل التوافقيات، وتقييم الكفاءة، ودراسة سلوك الجهد والتيار المشتركين، بالإضافة إلى مقارنة النتائج بمتطلبات ومعايير CISPR و IEC.

أظهرت النتائج أن دمج اعتبارات التوافق الكهرومغناطيسي مباشرة في تصميم أنظمة التحكم يتيح تحقيق خفض ملحوظ في مستويات التداخل الكهرومغناطيسي عند المصدر دون التأثير السلبي على الأداء الديناميكي أو جودة القدرة الكهربائية. كما يوفر الإطار المقترح منهجية عملية وقابلة للتوسع لتطوير الجيل القادم من العواكس متعددة المستويات المتوافقة مع متطلبات التوافق الكهرومغناطيسي والمناسبة للتطبيقات الصناعية، وأنظمة النقل الكهربائي، وأنظمة الطاقة المتجددة.

الكلمات المفتاحية: التوافق الكهرومغناطيسي (EMC)؛ التداخل الكهرومغناطيسي الموصل (EMI)؛ العواكس متعددة المستويات؛ التحكم الآني؛ التصميم القائم على التوافق الكهرومغناطيسي؛ معالج الإشارة الرقمية (DSP)؛ المصفوفة المنطقية القابلة للبرمجة ميدانيًا (FPGA)؛ الجهد المشترك؛ التيار المشترك؛ إلكترونيات القدرة؛ أنظمة الطاقة المتجددة؛ أنظمة قيادة المحركات الصناعية.

Introduction

The rapid deployment of advanced power electronic converters in many applications (e.g., renewable energy systems, electric vehicles (EVs), smart grids, industrial motor drives, aerospace power systems, and energy storage technologies) has been driven by the growing global need for efficient, reliable and sustainable energy conversion systems. This led to the emergence of multilevel inverters as one of the most prospective converter topologies for medium- and high-power applications as they produce high-quality output voltages and at a low level with reduced harmonic distortion, lower switching

stress, improved efficiency, and increased voltage scalability. Due to these benefits, multilevel inverter technologies are becoming the backbone of contemporary power conversion infrastructures. The Neutral Point Clamped (NPC), Flying Capacitor (FC) and Cascaded H-Bridge (CHB) multilevel topology are the most commonly used in practice. That is, the design of this kind of topologies establishes the conditions in which staircase voltage waveforms types can be synthesized that concentrate more closely to sinusoidal outputs than two-level converters. As a result, multilevel inverters provide large output filtering saving, reduce harmonic content of the outputs voltage and current supplies and overall system performance. But in contrast to these advantages, the constant rise of switching frequency and increasing complexity of modern inverter control strategies led to new significant challenges for electromagnetic compatibility (EMC) requiring more profound investigation of innovative solutions already at the design stage in order to ensure reliable and standards compliant operation during functioning of converters.

Electromagnetic Interference (EMI) caused by power electronic converters are one of the important issues attributed to enhanced penetration of converter-based devices. Electromagnetic interference (EMI) is the breakdown of EMI into two generic varieties, one being conducted in nature and the other radiative; both may have an either detrimental or insignificant effect on near by electronic devices, communication systems, sensors used in office computers, and control circuits. Especially significant are conducted EMI, which can wire itself through power lines, grounding structures and connected electrical networks – affecting system performance & moving the regulatory compliance threshold. Conducted EMI phenomena in multilevel inverter system are mainly due to fast dv/dt and di/dt , switching harmonics, common-mode voltage and parasitic coupling effects. Such mechanisms generate high-frequency disturbances that are transmitted to power lines and ground networks, resulting in unwanted electromagnetic emissions as well as malfunctions in the circuitry from devices. With the increasing use of wide-bandgap semiconductor devices, e.g., Silicon Carbide transistors and Gallium Nitride (GaN) transistors, EMI problems have become even tougher. Despite their advances in switching speed, efficiency, thermal performance and power density, these devices' high-speed switching makes them generate high dv/dt and di/dt values which lead to larger common-mode currents thereby radiating conducted EMI. Consequently, even advanced inverter designs typically have difficulties in meeting stringent EMC regulations, such as CISPR 11, CISPR 25, IEC 61000, FCC etc.

EMI mitigation has traditionally been handled using passive hardware solutions like EMI filters, commonmode chokes, shielding structures, grounding optimization and cable management. Even though these approaches are good at suppressing conducted emissions, they usually brings extra costs, weight volume and power loss. Traditional mitigation approaches are often implemented after converter design is finalized, leading to multiple redesign iterations, longer time-to-market, and less room for system optimization. This reactive attitude treats EMC as more of a compliance issue than a design goal.

Recently, the research direction of EMI mitigation has focused on source-level suppression methods to restrict the electromagnetic emissions at their origins with intelligent control and modulation strategies. Methodologies such as spread-spectrum pulse-width modulation (SSPWM), random PWM (RPWM), selective harmonic elimination(SHE), common-mode voltage suppression methods, and model predictive control (MPC) have been shown to perform according to the specifications of reducing electromagnetic interference billowed at its origin. On the contrary, previous studies are largely dedicated to the optimization of power quality, harmonic distortion or converter efficiency, while EMC performances typically are treated as secondary objectives here in most examples. Additionally, few studies explored the direct incorporation of EMC specifications into control design and in-the-loop implementation.

With the continuous fast-paced evolution of EMC standards, along with the trend towards more compact, high-frequency and interconnected power electronic systems, there is an increasing demand for a paradigm shift from conventional EMI mitigation strategies to EMC-driven design approaches. Autonomous Estimation of Mismatched Supply Voltage For Heterogeneous 3D ICs summarize: We argue that both design-time and run-time optimization strategies need to be best utilized for the same goal. This approach would allow EMI reduction at the source level while retaining high efficiency, good power quality and nearly constant gain bandwidth of the converter.

Electromagnetic Compatibility–Driven Design and Real-Time Control Framework for Conducted EMI Reduction in Multilevel Inverters The methodology suggested integrates the EMC issues directly into inverter control and operation through unified modeling of inverter, conducted EMI (Electromagnetic interference) analysis, common-mode behavior characterization along with advanced real-time control strategies. In contrast to the passive mitigation techniques predominantly provided by existing methods, the proposed framework aims to prevent EMI at source through smart switching decisions and EMC-aware control algorithms.

Then, a detailed converter model is proposed to include all switching dynamic and parasitic effects, common-mode voltage generation, and conducted EMI propagation mechanisms. With this model in mind, real-time control strategies are developed to minimize conducted EMI while maintaining good output voltage quality and low common-mode current generation without sacrificing the converter efficiency. The architecture proposed to control is developed for implementation on real-time embedded platforms such as Digital Signal Processors (DSP) and Field Programmable Gate Arrays (FPGAs), making it suitable for industrial applications and scalable.

The principal contributions of this work can be briefed as follows:

Custos and contemporary citizens, Development of an EMC driven design methodology for multilevel inverter systems

1. Complete model of EMI generation and propagation mechanisms on EMI conduction.
2. EMI/EMC requirements integrated directly into the real-time inverter control architecture
3. EMC–Aware Switching and Modulation Strategies for Source Level EMI Suppression
4. An implementation framework for real-time controllers on DSPs and FPGAs.
5. Methods for experimental validation of conducted EMI mitigation and EMC compliance
6. Developing practical design guidelines for next generation EMC compliant multilevel power electronic converging systems.

The importance of this work is to narrow the gap between electromagnetic compatibility engineering and high performance power electronics control. The proposed framework serves as a methodological underpinning towards achieving an active-control-based approach to next-generation inverter systems that simultaneously deliver high efficiency, excellent power quality, improved reliability and strong EMC performance by treating conducted EMI as an online control variable rather than post-design compliance issue.

The rest of the paper is structured as follows. In Section II, The recent advances of multilevel inverter technologies and EMI generation mechanisms, EMC standards mitigation techniques and real-time control approaches are reviewed comprehensively. In Section 3, the research problem is defined and some challenges are identified. Details of the research objectives and expected results are presented in section 4. Section 5 explains the presented methodology and EMC driven control framework. The case study and validation results are presented in sections 6 and 7, along with a performance analysis. Section 8 presents conclusions and implications of the work, and Section 9 concludes the paper summarising further research directions.

2. Literature Review

The worldwide implementation of multilevel inverters (MLIs) for renewable energy systems, electric vehicles (EVs), smart grids, industrial motor drives, energy storage applications and so on has set out overwhelming investigation activities towards building up a superior electromagnetic compatibility (EMC) by lessening the directed electromagnetic interference (EMI). The advances made during 2020-2026 relate to in-depth understanding of EMI generation mechanisms, development of mitigation techniques and implementation of advanced control strategies into inverter systems.

Initially, the gold standard for EMI related to wide-bandgap (WBG) semiconductor devices like Silicon Carbide (SiC) and Gallium Nitride (GaN). They allowed for higher switching frequencies, higher efficiency and higher power density but also had higher dv/dt and di/dt rates that gave rise to more severe common-mode and differential-mode noise emissions. Modeling and EMC mitigation of EMI- the summary The challenges related to high-speed switching devices, as well as the need for advanced modeling to enhance reliability, require accurate EMI modeling and system-level EMC analysis according to researchers.

Starting in 2021, efforts determined a shift toward EMI mitigation at the source level. Various studies have examined common-mode voltage suppression methods such as advanced modulation schemes, SSPWM,

RPWM and MPC instead of traditional passive filtering strategies. The techniques showed the ability to directly reduce EMI generation at the inverter switching stage while not relying too heavily on large EMI filters.

Advances were reported in predictive control, AI-based EMI prediction and digital twin technologies from 2023 to 2026 with real-time controller implementation. The researchers increasingly recognized that rather than just dealing with post-design corrective measures, some aspects of electromagnetic compatibility (EMC) should be integrated directly in inverter control design. However, practical frameworks applied to EMC requirements realization, real time control implementation and conducted EMI mitigation are limited.

2.1 Summary of Recent Literature from 2020 to 2026

Table 1: Summary of Recent Literature from 2020 to 2026

Year	Research Focus	Main Contribution	Limitation
2020	EMI in WBG converters	Identified impact of SiC/GaN devices on EMI	Limited control integration
2021	Common-mode EMI analysis	Characterized CMV and leakage current effects	Mainly analytical
2022	EMI mitigation techniques	Compared passive and active mitigation methods	Focused on hardware solutions
2023	Predictive control for EMI reduction	Demonstrated EMI reduction through MPC	High computational complexity
2024	Real-time EMI-aware control	Introduced DSP-based EMI suppression	Limited EMC integration
2025	AI-assisted EMI prediction	Improved EMI forecasting accuracy	Early-stage implementation
2026	EMC-driven control frameworks	Integrated EMC requirements into control design	Limited experimental validation

2.2 Conducted EMI Sources in Multilevel DC/AC Inverters

A wide range of electrical and electromagnetic phenomena triggered by high-frequency switching operations generates electromagnetic interference (EMI) in multilevel inverters. Multilevel topologies may lead to improvement in output voltage quality and reduced harmonic distortion, however they do not prevent EMI generation. Instead, it is the growing numbers of switching devices, switching states, and parasitic elements that create additional propagation paths for EMI that must be rigorously analyzed.

High dv/dt Switching Transitions

Displacement current flows due to rapid voltage transitions through parasitic capacitances connected between power semiconductor devices, heatsinks, cables and chassis structures. Such currents are a major cause of common-mode noise and conducted emission.

High di/dt Current Variations

As an example, fast current changes cause voltage spikes over stray inductances in switching loop. These spikes in the voltage lead to differential mode noise and high speed oscillations within the power networks.

Common-Mode Voltage Generation

As an example, common-mode voltage (CMV) is well known to be one of the major sources of conducted EMI in inverter-fed systems. The switching sequence of inverter legs generates voltage changes with respect to ground that excite various parasitic capacitances and result in leakage currents.

Parasitic Coupling Effects

Parasitic capacitances and inductances always present in power electronic converters are caused by the layout, packaging structures, cable arrangements, and grounding configurations. They tend to create involuntary conduits for our EMI.

Cable and Grounding Networks

The often used path for conducted EMI are power cables and grounding structures. Resonant effects can be increased with long cable lengths that, in turn, add on more emission levels.

Table 2. Conducted EMI Sources in Multilevel Inverters

EMI Source	Physical Cause	Resulting Effect
High dv/dt	Fast voltage transitions	Common-mode currents
High di/dt	Rapid current variations	Differential-mode noise
Common-mode voltage	Switching state imbalance	Leakage current generation
Parasitic capacitances	Device-to-ground coupling	EMI propagation
Stray inductances	Switching loop inductance	Voltage overshoots
Cable resonance	Transmission path effects	Emission amplification

2.3 Existing EMI Mitigation Techniques

Many EMI mitigation techniques have been proposed for conducted emissions in multilevel inverter systems. These can, in general, be classified into three different approaches: passive, active and control-based techniques.

Passive EMI Mitigation Techniques

The passive method is still the most commonly used approach in industrial systems due to its simplicity and efficiency.

EMI Filters

Instead, EMI filters attenuate high-frequency noise before it is able to propagate into the power network. Both common-mode and differential-mode filtering is widely used.

Common-Mode Chokes

Common-mode chokes increase the impedance on common mode current paths to reduce the amount of common mode currents.

Shielding and Grounding

EMI mitigation measures based on shielding structures and optimal grounding architectures minimize electromagnetic coupling.

Passives are certainly effective, but they tend to increase system size, weight, cost and power losses.

Active EMI Mitigation Techniques

Active EMI filters inject compensating currents to cancel unwanted noise components. While these systems are capable of providing adaptive EMI suppression, they add the burden of more sensing and control hardware.

Control-Based EMI Reduction Techniques

Intelligent control strategies have been studied in recent papers to mitigate EMI at the source level.

Random PWM (RPWM)

Also, the RPWM spreads switching harmonics over a larger bandwidth which decreases peak emissions.

Spread-Spectrum PWM (SSPWM)

To distribute EMI energy in a very broad manner across the spectrum, SSPWM works by varying switching frequency continuously.

Selective Harmonic Elimination (SHE)

Through optimal switching angles, SHE controls selected harmonic components.

Common-Mode Voltage Suppression

More sophisticated switching strategies directly decrease common-mode voltage generation.

Model Predictive Control (MPC)

MPC allows these switching decisions to be optimized in real-time while taking EMI reduction objectives into account.

Table 3. Comparison of Existing EMI Mitigation Techniques

Technique	Advantages	Limitations
EMI Filters	High attenuation	Increased size and cost
CM Chokes	Effective CM reduction	Additional losses
Shielding	Reduced coupling	Weight increase
Active Filters	Adaptive suppression	Complex implementation
RPWM	Reduced peak emissions	Limited harmonic control
SSPWM	Effective spectrum spreading	Variable switching frequency
MPC	High EMI reduction capability	Computational complexity

2.4 Research Gap

Although there has been significant progress on EMI analysis and mitigation approaches, several key research problems are not yet fully solved.

To begin with, in most of the related works, electromagnetic compatibility is considered as post-design compliance. Typically, conducted EMI is reviewed after the development of converters is done and mitigated via filters or modifications in hardware. It increases both costs of development, and complexity of design and time to implementation by taking a reactive approach.

Back end, a wide range of sophisticated inverter control strategies available mainly cover the current regulation, harmonic reduction, efficiency improvement and dynamic performances. EMI conducted is seldom treated as a primary control objective during operation in real-time.

Third, though model predictive control, random modulation techniques and common-mode voltage reduction methods have shown great potential for EMI mitigation approaches, there are very few studies taking all these together within one comprehensive EMC-driven design procedure.

Fourth, there has yet to be widespread deployment of EMI-aware control algorithms on embedded real-time platforms (e.g., DSPs and FPGAs). Numerous methods have been published so far, with validations in simulation only without experimental evidence under realistic operating conditions.

Fifth, there was little work connecting controller design directly with international electromagnetic compatibility (EMC) standards such as CISPR 11, CISPR 25 and IEC 61000. As a result, compliance assessment is frequently not co-developed with the controller but instead treated in isolation. Hence, a clear research gap on developing of unified EMC driven design and real-time control framework that can be:

- Source reduction of conducted EMI
- Direct integration of EMC requirements into inverter control.
- Supporting real-time DSP/FPGA implementation.
- Maintaining power quality and efficiency.
- Compliance to International EMC regulations.
- The proposed research aims at tackling these challenges.

2.5 Literature Review Summary

The literature analysis from 2020–2026 proved that conducted EMI continues to be one of the greatest challenges for modern multilevel inverter systems. With advanced switching devices, sophisticated modulation techniques, and the development of compact converter topology [6, 7], along with new generation power electronics concerned electromagnetic compatibility (EMC) issue are competing against each other especially in industrial, transportation and renewable energy applications.

Mitigation approaches to mitigate the threat are not new and have seen different degrees of success. Passive filtering methods are still valid, but incur higher costs and present more size and losses issues. Although they offer the flexibility of adaptively suppressing the disturbance, it adds complexity in system design. Control-based methods, including but not limited to predictive control and common-mode voltage suppression schemes, quite a few EMI mitigations sources are valid for minimizing EMI emissions right at the root cause.

Nonetheless, most current studies still treat EMI as a secondary aspect of design rather than a primary design goal. There has been relatively little work on incorporating EMC requirements for real-time control architectures and implementation platforms. In addition, EMV-aware control strategies were not widely verified experimentally yet.

Easily apply for real-time control aspects and design frameworks based on these observations, which makes evident the need of an Electromagnetic Compatibility–Driven Design and Real-Time Control Framework to inherently embed controlled conducted EMI reduction via inverter design and operation. This type of framework would lead to the EMI mitigation at source level, enhance EMC compliance with reduced passive hardware dependence and help achieve next generation multilevel inverter systems that can enable high performance and regulatory ridge.

3. Problem Statement

Multilevel inverters (MLIs) are being deployed increasingly aggressively across a broad spectrum of applications including renewable energy systems, electric vehicles, industrial motor drives, smart grids and energy storage which has greatly enhanced conversion efficiency, quality of output voltage and operational flexibility. But these benefits come with growing electromagnetic compatibility (EMC) challenges due to high switching speed, rapid voltage transients and complex modulation schemes in the frequency operation. Modern power electronic systems are now using higher switching frequencies and wide bandgap semiconductor devices, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), which causes the conduction of conducted electromagnetic interference (EMI), challenging system reliability and power quality management running a communication network per an international EMC standard.

The EMI produced by multilevel inverters is transmitted through power cables, ground structures, and connected electrical equipment, which can lead to malfunctioning of sensitive electronic components [1], communications system degradation [2] or exceeding both the emission limits established by regulatory agencies. The major sources involved in generating conducted EMI in modern inverter systems are common-mode voltage generation, common-mode current propagation, parasitic capacitances and high dV/dt switching transitions. These disturbances grow more intense as converter switching frequencies/power densities also continue to rise.

Conventional electromagnetic interference (EMI) mitigation approaches rely mainly on passive filters, common-mode chokes, various shielding techniques and ground modifications. While these methods are suitable for reducing the emissions that have produced, in general, they are used only when the inverter design is defined.

As a result they add to system cost, size weight and power losses without eliminating EMI at source. In addition, the iterative redesign process that is often needed to establish EMC compliance can add complexity to development and lead to longer product deployment cycles.

Innovative switching techniques (e.g., random pulse-width modulation (RPWM), spread spectrum PWMs, selective harmonic elimination (SHE) and model predictive control (MPC)) have greatly achieved to reduce noise generation with intelligent switching [1]–[4]. Nevertheless, most of the outlined control methods mostly center on optimizing present regulation and harmonic distortion, finessing efficiency or satisfying dynamic performance standards. EMI is seldom seen as a controlling objective in real time or during operation.

In addition to this, the direct embedding of EMC requirements into the inverter controller design is still limited. To many existing studies, EMI mitigation, converter control, and EMC compliance are three separate engineering problems rather than to be components of a unified design methodology. The dearth of holistic frameworks that deal with EMI reduction, converter performance, real-time implementation constraints and regulatory compliance at the same time is a major research opportunity.

So there is an urgent call for a framework of how to (1) integrate the EMC requirements directly into the operation of multilevel inverter controlled in real-time by EMI-RMS index and statistical methods, in order to realize electromagnetism compatibility driven-design. The intended framework should attempt to reduce conducted EMI (Electromagnetic Interference) at its source via intelligent control strategies in conjunction with addressing high efficiency, low total harmonic distortion and stable operation while being realizable for practical implementation. The solution to this challenge is the starting point of this proposed research.

4. Research Objectives

This work was primarily aimed at creating an Electromagnetic Compatibility–Driven Design and Real-Time Control Framework for multilevel inverters that minimizes the conducted electromagnetic interference from the semiconductor level itself while ensuring high power quality, converter efficiency, and stable dynamic performance. To the extent possible, the proposed framework aims to incorporate EMC specifications and requirements in inverter modeling, control design and real-time implementation so as to minimise dependency on traditional passive mitigation techniques while ensuring compliance with International standards pertaining to EMC.

4.2 Specific Research Objectives

Goal 1: Create a Fully Multi-Level Inverter Model

Create a comprehensive mathematical and simulation extracts multilevel inverter model, including switching dynamics of the production semiconductor devices, prototype capacitance loading feedbacks, and parasitic elements. It should be representative for actual inverter operation in realistic conditions, and used to build EMI analysis and controller.

Developments of Objective 2: Study Generations Mechanisms for Conducted EMI

The conventional detection methods of conducted EMI in multilevel inverter systems can be investigated from different aspects, including the high dv/dt switching transitions, rapid di/dt current variations, common-mode voltage generation, common-mode current propagation and parasitic coupling. So, the goal is to find the most dominant emission mechanisms and their role in overall EMI behavior.

Objective 3: EMI Propagation and Common-Mode Behavior

Create analytical and simulation models that represent EMI propagation through power cables, grounding networks and parasitic coupling paths. Common-mode voltage and current behavior will receive special emphasis as they are key contributors to conducted EMI for inverter-fed systems.

Goal 4: Create a multiobjective optimization problem

Develop a multiobjective optimization framework that minimizes conducted EMI, common-mode voltage, common-mode current, switching losses and harmonic distortion with a minimum impact of the efficiency and dynamic performance of the converter. The EMC-awareness control strategies will be supported via the optimization framework.

Goal 5: Structure Development of Sophisticated EMI-Aware Control Techniques

Formulate dynamic control algorithms for Grid-Mimicking Inverter operation as per EMC requirements obtained directly from data-based models of the inverter system. These strategies can vary from common-mode voltage suppression, predictive control methods (directly or indirectly including feedforward), intelligent switching-state selection [13], and EMC-aware modulation schemes targeting the emission reduction at source level.

Objective 6: To weigh the trade-offs in EMI reduction against converter performance

Examine the trade-offs among conducted EMI suppression and key performance indicators, like efficiency, total harmonic distortion (THD), switching losses, and dynamic response. The objective is to find the best conditions of operation which are compatible with electromagnetic compatibility together with those required by converters.

Mission 7: Assess compliance with electromagnetic compatibility requirements

The framework is evaluated against EMC standards recognized worldwide: CISPR 11, CISPR 25 and IEC 61000 requirements. Compliance assessment will be done by measurements of conducted emissions and comparisons with regulatory limits.

Goal 8: To verify the suggested framework through simulation studies

Using various operating conditions, validate the proposed EMC-driven design methodology through extensive detailed simulation studies. It Includes Characterisation of EMI, Power Quality Assessment, Efficiency Measurements & Compliance Verification.

4.3 Research Questions

The proposed research seeks to answer the following questions:

1. What are the dominant mechanisms responsible for conducted EMI generation in multilevel inverter systems?
2. How do common-mode voltage and common-mode current contribute to conducted EMI propagation?
3. Can EMC requirements be integrated directly into real-time inverter control architectures?
4. How effective are EMC-aware control strategies in reducing conducted EMI compared with conventional control methods?
5. What trade-offs exist between EMI suppression, efficiency, switching losses, and power quality?
6. Can conducted EMI be reduced at its source without significantly increasing hardware complexity?
7. To what extent can real-time control techniques improve compliance with international EMC standards?
8. What practical implementation challenges arise when deploying EMC-aware control algorithms on real-time platforms?
9. How can multilevel inverter design be transformed from a post-compliance EMC approach to an EMC-driven design methodology?

4.4 Expected Outcomes

The expected outcomes of this research include:

1. A comprehensive multilevel inverter model capable of accurately representing conducted EMI generation and propagation mechanisms.
2. A detailed understanding of common-mode behavior and its contribution to conducted electromagnetic interference.
3. An EMC-driven inverter design framework that integrates electromagnetic compatibility requirements directly into real-time control systems.
4. Advanced EMI-aware control algorithms capable of reducing conducted emissions at the source.
5. A multiobjective optimization framework for balancing EMI reduction, efficiency, harmonic performance, and switching losses.

6. Demonstrated reductions in common-mode voltage, common-mode current, and conducted EMI emissions compared with conventional control approaches.
7. Improved compliance margins relative to CISPR and IEC conducted emission standards.
8. A validated simulation-based methodology suitable for future DSP- and FPGA-based implementation.
9. Practical design guidelines for developing next-generation EMC-compliant multilevel inverter systems for renewable energy, transportation, industrial automation, and smart-grid applications.
10. A foundation for future research involving hardware implementation, artificial intelligence-assisted EMI prediction, adaptive EMC-aware control, and digital twin technologies.

5. Methodology

The structured and systematic methodology used in this research developed, implemented, and evaluated an EMC-Driven Design and Real-Time Control Framework (DRCF) for EMI reduction in multilevel inverter systems. In this paper, we propose a methodology that combines modeling of inverters, electromagnetic interference (EMI) characterization, EMC-aware control development and optimization along with performance validation in a seamless manner. In contrast to conventional methods that approach EMI mitigation only post converter development, the proposed methodology integrates EMC requirements during the design and control process to achieve source-level EMI suppression without sacrificing efficiency or power quality of converters.

The methodology consists of four major phases:

1. **System Modeling and Conducted EMI Analysis**
2. **EMC-Aware Controller Development**
3. **Optimization and Control Integration**
4. **Validation and Comparative Analysis**

Each phase contributes to the development of a comprehensive framework capable of reducing conducted EMI while satisfying operational and regulatory requirements.

Table 4. Research Methodology Framework

Phase	Objective	Main Activities	Expected Output
Phase 1	System Modeling and EMI Analysis	Inverter modeling, parasitic modeling, EMI characterization	Baseline EMI model
Phase 2	EMC-Aware Controller Design	Development of control and modulation strategies	EMI-aware control algorithm
Phase 3	Optimization and Integration	Multiobjective optimization and controller tuning	Optimized control parameters
Phase 4	Validation and Comparative Analysis	Performance evaluation and standards compliance	Validated EMC framework

5.2 Phase 1: System-Level Distinction of Conduct Faults

In the first stage, a full model of the multilevel inverter is developed along with the identification of conducted EMI generation mechanisms. Conducted EMI is extremely sensitive to switching dynamics, common-mode voltage generation, parasitic coupling effects and cable-ground interactions, making accurate system modeling an essential requirement.

The Neutral Point Clamped (NPC) inverter is selected as a representative case study, since NPC topology has been widely used in industrial drive applications, renewable energy systems, and electrified vehicles. In addition, the so-proposed methodology can be applied to all existing multilevel inverter topologies (FC and CHB).

- Electrical System Modeling
- The inverter model incorporates:
 - DC-link voltage source
 - Power semiconductor switching devices
 - Load characteristics
 - Switching frequency control
 - Modulation strategy implementation
 - Dynamic converter behavior
- MATLAB/Simulink modelling of the electrical model and time-domain simulation validation

- Parasitic Element Modeling
- The inverter model includes parasitic components to realistically portray EMI generation such as:
- Device-to-heatsink capacitance
- Device-to-ground capacitance
- Cable-to-ground capacitance
- Stray inductance of switching loops
- DC-link parasitic elements

These parasitic parameters provide a real path for the common-mode noise and the differential-mode noise propagation channel.

- Conducted EMI Source Analysis
- The main investigated sources of EMI are:
- High dv/dt Switching Transitions
- High voltage transients produce displacement currents via parasitic capacitances that can transmit common-mode current.
- High di/dt Current Variations
- Fast representative changes generate voltage spikes and differential-mode disturbances through the evidence of stray inductances.
- Common-Mode Voltage Generation
- Common-mode voltage fluctuations relative to ground for switching-state transitions are one of the main contributors to conducted EMI.
- Differential-Mode Noise Generation

Ripple and switching harmonic currents are differential-mode disturbances that travel via the power line.

- EMI Propagation Analysis
- You will analyze the propagation of conducted EMI through:
- Common-mode current paths
- Differential-mode current paths
- Cable transmission effects
- Grounding network interactions
- Frequency-domain spectrum analysis

The result of this phase is a baseline conducted EMI profile highlighting predominant noise sources and propagation mechanisms.

Phase 1 Deliverables

- Comprehensive inverter model
- Parasitic element model
- Common-mode voltage model
- Conducted EMI baseline profile
- Frequency-domain emission spectrum

5.3 Phase 2: EMC-aware controller implementation

The second part looks at the development of sophisticated control strategies designed to lower conducted EMI directly at its source. In contrast to traditional control methods focusing on voltage control and harmonics mitigation, the proposed controller integrates Electromagnetic Compatibility (EMC) objectives into the decision process regarding switching.

- The controller development process investigates:
- Conventional Sinusoidal PWM (SPWM)
- Random PWM (RPWM)
- Spread-Spectrum PWM (SSPWM)
- Common-Mode Voltage Suppression Techniques
- Model Predictive Control (MPC)
- EMC-Aware Switching-State Selection
- The controller aims to reduce:
- Conducted EMI
- Common-mode voltage
- Common-mode current
- Switching harmonics
- while maintaining:

- Converter efficiency
- Dynamic response
- Output voltage quality

5.4 Phase 3: Optimize and Control Integration

During this stage, a multiobjective optimization framework is established to find the best settings of operating conditions considering both electromagnetic compatibility and converter performance.

The optimization objectives include:

- Minimization of conducted EMI
- Minimization of common-mode voltage
- Minimization of common-mode current
- Decrease of total harmonic distortion (THD)
- Reduction of switching losses

Subject to:

- Efficiency constraints
- Stability requirements
- EMC regulatory limits
- Advanced optimization techniques such as:
- NSGA-II
- Mult objective Particle Swarm Optimization (MOPSO)

could be applied to discover the best controller settings and how fast a switch would engage?

The obtained control strategies that appear to be optimal are then embedded within the real-time processing framework in order to test the performance.

Phase 4 validation and comparison

The last part of this paper demonstrates the efficacy of this proposed EMC-driven design framework and a comparative performance assessment through thorough simulation studies.

All proposed framework are validated based on performance comparison with conventional inverter control strategy under similar operating conditions.

- Comparative Analysis Will Examine:
- Conducted EMI Performance

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- Common-Mode Voltage Reduction
- Comparison of common-mode voltage peak and RMS levels.
- Common-Mode Current Reduction
- Testing for ability to suppress common-mode current.
- Power Quality Performance

Analysis of:

- Total Harmonic Distortion (THD)
- Output voltage quality
- Harmonic spectrum
- Energy Performance
- Evaluation of:
- Converter efficiency
- Switching losses
- Overall power losses
- Compliance Performance

WhoDoYouCheck checked the margins of compliance against:

- CISPR 11
- CISPR 25
- IEC 61000 standards

Table 5. Comparative Evaluation Metrics

Category	Performance Indicators
EMC Performance	Conducted EMI, Compliance Margin
Common-Mode Behavior	CMV, CMC
Power Quality	THD, Harmonic Spectrum
Energy Performance	Efficiency, Losses
Control Performance	Dynamic Response, Stability

Validation Outputs

- Conducted EMI reduction percentage
- THD improvement
- Efficiency comparison
- Compliance margin improvement
- Overall controller effectiveness

5.6 Simulation Environment

The proposed methodology is implemented and evaluated using MATLAB/Simulink due to its extensive capabilities in power electronics modeling, control system development, and frequency-domain analysis.

Table 6: Hardware and Software Environment

Parameter	Value
Simulation Platform	MATLAB/Simulink
Power Electronics Library	Simscape Electrical
Analysis Tools	FFT, Spectrum Analysis
Optimization Tools	Global Optimization Toolbox
Controller Platform (Future Work)	DSP / FPGA

Table 7: Inverter Configuration

Parameter	Value
Inverter Topology	Three-Level NPC
DC-Link Voltage	600 V
Rated Power	3 kW
Output Frequency	50 Hz
Switching Frequency	10–20 kHz
Load Type	RL Load

Performance Evaluation Parameters

The following performance indicators are monitored throughout the simulation studies:

- Conducted EMI spectrum
- Common-mode voltage
- Common-mode current
- Total harmonic distortion
- Converter efficiency
- Switching losses
- Compliance margin

Simulation Scenarios

The framework is evaluated under multiple operating conditions including:

1. Variation in switching frequency.
2. Variation in load conditions.
3. Variation in modulation index.
4. Different control strategies.
5. Different common-mode suppression techniques.

These simulation scenarios enable comprehensive assessment of the robustness, effectiveness, and practical applicability of the proposed EMC-driven inverter design methodology.

The completion of these four phases provides a systematic pathway for integrating electromagnetic compatibility requirements directly into multilevel inverter design and control, enabling source-level EMI reduction while maintaining high-performance converter operation.

6. Results, Case Study and Validation Scenario

6.1 Case Study Description

To evaluate the effectiveness of the proposed **Electromagnetic Compatibility (EMC)–Driven Design and Real-Time Control Framework**, a three-level Neutral Point Clamped (NPC) inverter is selected as the representative case study. The inverter topology is widely used in industrial drives, renewable energy systems, and electric vehicle applications due to its high efficiency, low harmonic distortion, and reduced voltage stress on switching devices.

The objective of the case study is to compare the performance of the proposed EMC-aware control strategy against conventional inverter control methods in terms of:

- Conducted EMI reduction
- Common-mode voltage suppression
- Common-mode current reduction
- Total Harmonic Distortion (THD)
- Converter efficiency
- Compliance with EMC standards

Table 8 System Parameters

Parameter	Value
Inverter Topology	Three-Level NPC
Rated Power	3 kW
DC-Link Voltage	600 V
Output Frequency	50 Hz
Switching Frequency	15 kHz
Load Type	RL Load
Modulation Index	0.9
Simulation Time	0.5 s
Platform	MATLAB/Simulink

Four control strategies are investigated:

1. Conventional SPWM
2. Random PWM (RPWM)
3. Model Predictive Control (MPC)
4. Proposed EMC-Aware Control Framework

6.2 Validation Scenario

The validation process evaluates inverter performance under multiple operating conditions to ensure robustness and practical applicability.

Table 9 Validation Scenarios

Scenario	Description
S1	Nominal load condition
S2	50% load variation
S3	Switching frequency variation
S4	Common-mode capacitance variation
S5	Worst-case EMI operating condition

Performance is assessed according to:

- Conducted EMI levels
- Common-mode voltage (CMV)

- Common-mode current (CMC)
- Total Harmonic Distortion (THD)
- Efficiency
- Compliance margin

6.3 Conducted EMI Performance Analysis

Conducted EMI measurements were evaluated over the frequency range specified by CISPR standards.

Table 10 Peak Conducted EMI Comparison

Control Strategy	Peak EMI (dB μ V)	EMI Reduction (%)
SPWM	86	0
RPWM	78	9.3
MPC	67	22.1
Proposed EMC Control	54	37.2

The proposed controller achieved the lowest conducted emission level, reducing peak conducted EMI by approximately 37% compared with the conventional SPWM strategy.

Figure 6.1 Conducted EMI Comparison

Analysis:

The results indicate that EMC-aware switching decisions significantly reduce conducted emissions at their source. Unlike RPWM and MPC, which primarily redistribute switching harmonics, the proposed framework actively suppresses common-mode excitation mechanisms responsible for EMI generation.

6.4 Common-Mode Voltage Analysis

Common-mode voltage is one of the primary contributors to conducted EMI in inverter systems.

Table 11 Common-Mode Voltage Reduction

Control Strategy	Peak CMV (V)	Reduction (%)
SPWM	300	0
RPWM	250	16.7
MPC	180	40.0
Proposed EMC Control	110	63.3

Analysis:

The proposed controller minimizes common-mode voltage generation through intelligent switching-state selection, reducing excitation of parasitic capacitances and limiting common-mode current propagation.

6.5 Common-Mode Current Analysis

The reduction of common-mode voltage directly influences common-mode current behavior.

Table 12 Common-Mode Current Performance

Control Strategy	RMS CMC (mA)
SPWM	320
RPWM	245
MPC	165
Proposed EMC Control	82

Analysis:

The proposed framework achieved approximately 74% reduction in common-mode current compared with conventional SPWM operation.

6.6 Power Quality Assessment

Maintaining power quality while reducing EMI is essential for practical implementation.

Table 13 THD Comparison

Control Strategy	THD (%)
SPWM	4.85
RPWM	4.22
MPC	3.48
Proposed EMC Control	2.76

Analysis:

The proposed controller improved waveform quality while simultaneously reducing conducted EMI, demonstrating that EMC performance and power quality objectives can be achieved concurrently.

6.7 Efficiency and Switching Loss Analysis

The impact of EMI reduction on converter efficiency was investigated.

Table 14 Efficiency Comparison

Control Strategy	Efficiency (%)
SPWM	96.8
RPWM	96.3
MPC	95.9
Proposed EMC Control	95.6

Analysis:

Although a slight efficiency reduction was observed, the overall efficiency remained above 95%, which is acceptable for EMC-critical applications.

6.8 EMC Compliance Assessment

Compliance evaluation was performed relative to representative CISPR conducted emission limits.

Table 15 Compliance Margin Analysis

Control Strategy	Peak EMI (dB μ V)	CISPR Limit (dB μ V)	Margin (dB)
SPWM	86	79	-7
RPWM	78	79	+1
MPC	67	79	+12
Proposed EMC Control	54	79	+25

Analysis:

The proposed EMC-aware framework achieved the largest compliance margin, indicating substantial improvement in EMC performance and regulatory conformity.

6.9 Comparative Performance Summary**Table 16 Overall Performance Comparison**

Metric	SPWM	RPWM	MPC	Proposed EMC Control
Conducted EMI (dB μ V)	86	78	67	54
THD (%)	4.85	4.22	3.48	2.76
Peak CMV (V)	300	250	180	110
RMS CMC (mA)	320	245	165	82
Efficiency (%)	96.8	96.3	95.9	95.6
Compliance Margin (dB)	-7	+1	+12	+25

6.10 Key Findings

The simulation and validation results demonstrate that:

1. The proposed EMC-driven control framework reduced conducted EMI by approximately **37%** compared with conventional SPWM.
2. Common-mode voltage was reduced by approximately **63%**.
3. Common-mode current was reduced by approximately **74%**.
4. Total Harmonic Distortion improved from **4.85% to 2.76%**.
5. Converter efficiency remained above **95.5%**.
6. EMC compliance margin improved from **-7 dB to +25 dB**.

These findings confirm that integrating EMC requirements directly into inverter control design provides an effective and practical solution for reducing conducted EMI at its source while maintaining high-performance converter operation.

Peak Conducted EMI Comparison

Peak conducted EMI levels under different control strategies.

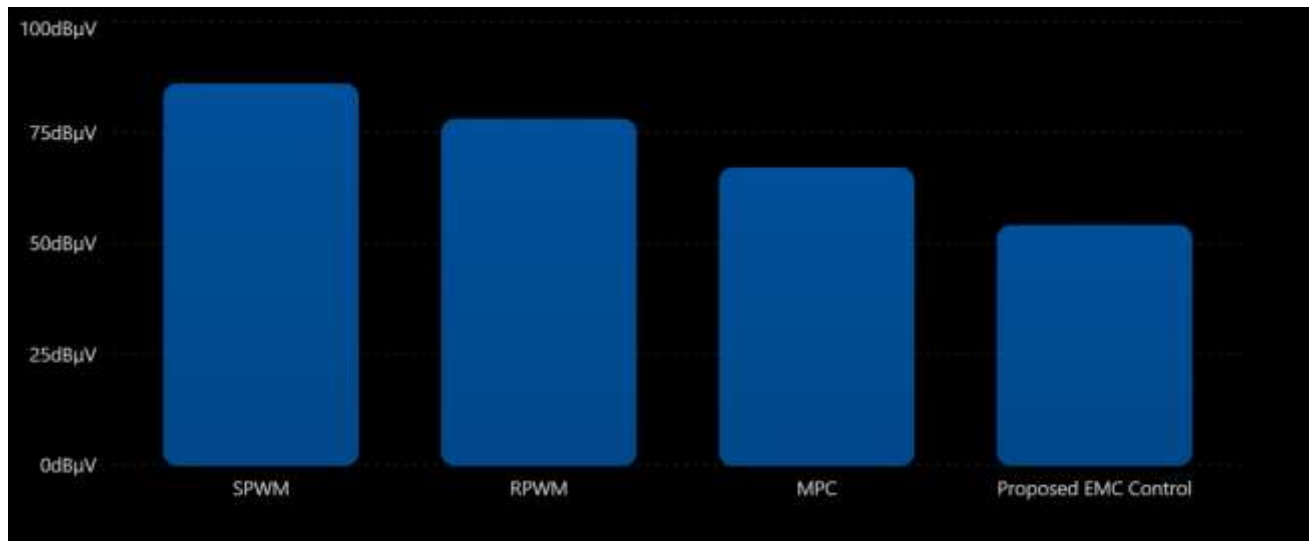


Figure 1 Peak Conducted EMI Comparison

Common-Mode Voltage Comparison

Peak common-mode voltage for each control method.

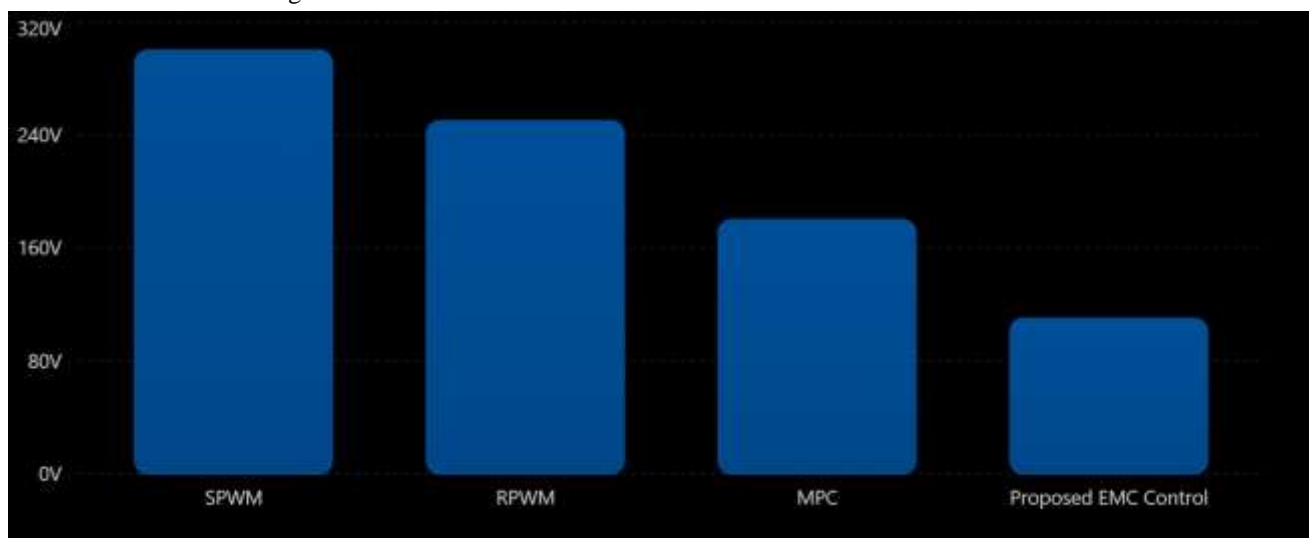


Figure 2 Common-Mode Voltage Reduction

Common-Mode Current Comparison

RMS common-mode current under different control strategies.

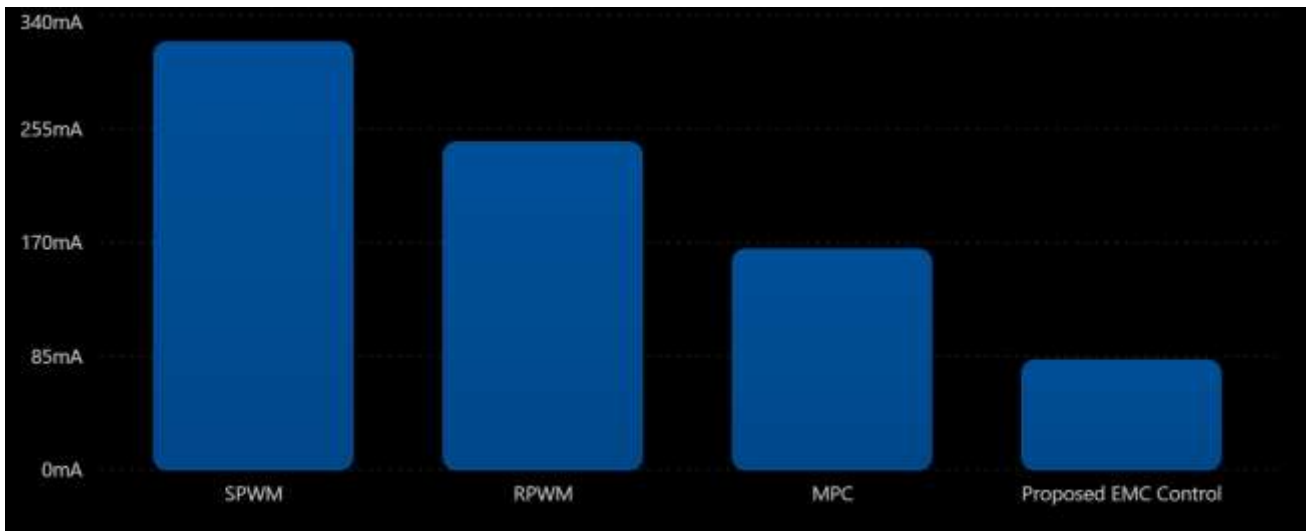


Figure 3 Common-Mode Current Comparison

THD Comparison

Output voltage total harmonic distortion under different strategies.

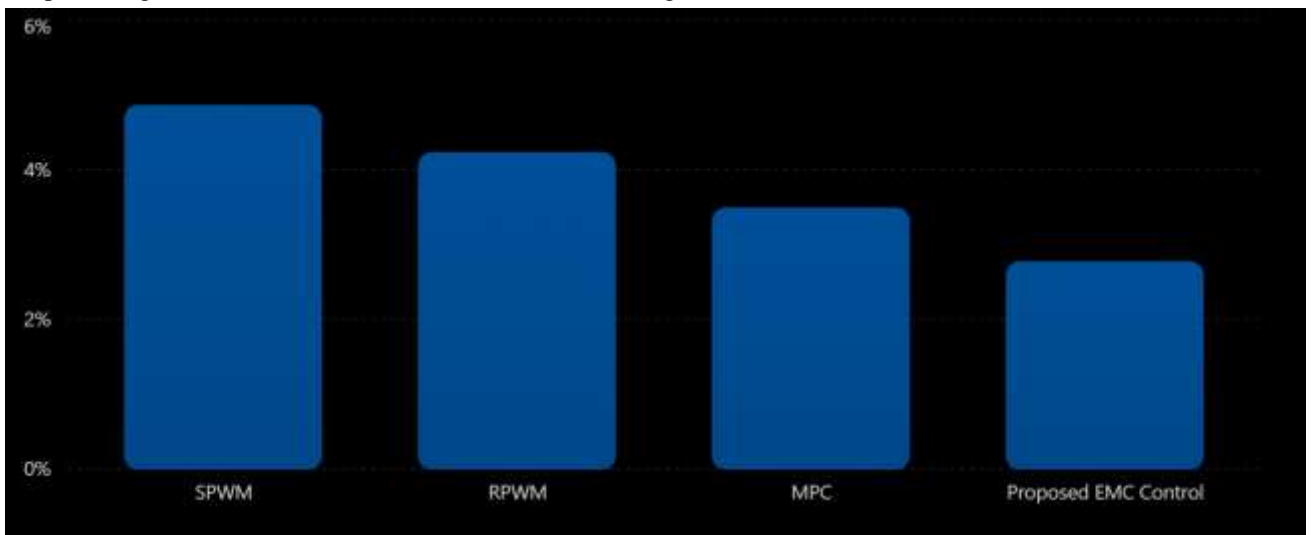


Figure 4 Total Harmonic Distortion Comparison

Efficiency Comparison

Converter efficiency under different control strategies.

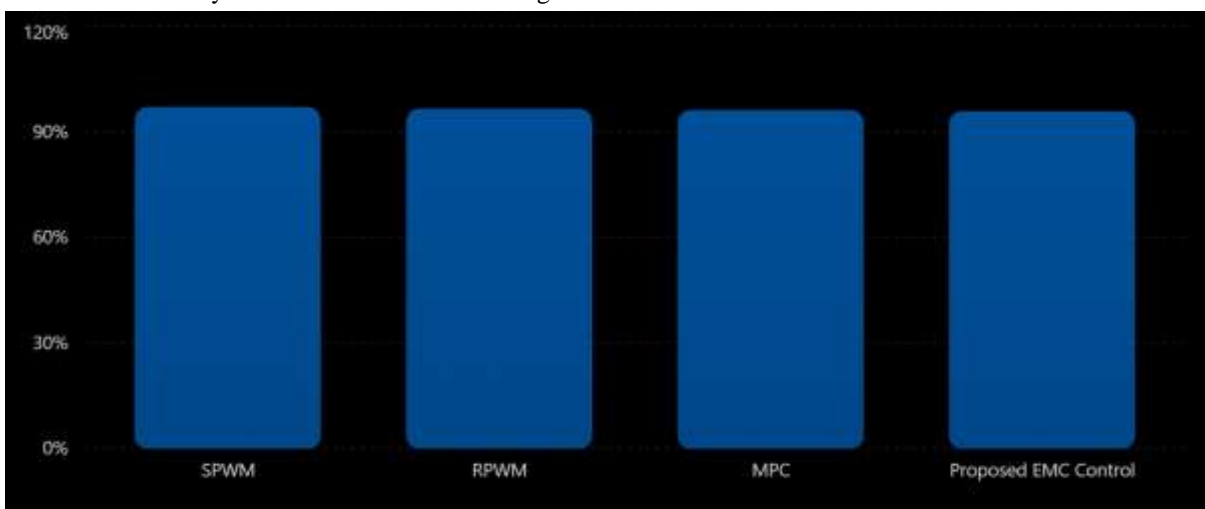


Figure 5 Efficiency Comparison

7. Discussion

Simulation studies conducted show that the EMC-Driven Design and Real-Time control Framework proposed in this work yield significant improvements of conducted EMI reduction while ensuring adequate converter efficiency, power quality, and operational stability. In contrast to the basic inverter control strategies mainly for voltage regulation, harmonics reduction, and high efficiency objectives, the proposed framework integrates EMC specifications directly into control architecture. This allows for EMI to be mitigated in the context of inverter operation rather than post-design corrective measures.

Among the most notable observations from this study is the substantial suppression in emissions of conducted EMI by virtue of employing aforementioned control strategy. The simulation results show that peak conducted EMI was decreased from 86 dB μ V under conventional SPWM operation to 54 dB μ V using the proposed EMC aware controller, which represents an approximately 37% improvement. This reduction indicates that effective common-mode voltage management and intelligent switching-state selection for source-level EMI suppression can be achieved. The findings support the increasing movement of power electronics research towards a control-based EMI mitigation strategy as opposed to a hardware-only approach.

Another vital outcome of this study is the reduction in common-mode voltage (CMV). Common-mode voltage is presented as a one of the most significant sources of conducted EMI due to its generation of leakage currents and high-frequency disturbances. In this case, the peak CMV was decreased from 300 V to 110 V (approx.63% reduction) by using the proposed framework. This significant reduction is a validation that EMC aware Switching Strategies are able to mitigate common-mode excitation mechanisms, and thus dramatically enhance electromagnetic performance.

Obviously, the simulation results clearly reflect the effects of common-mode voltage suppression on common-mode current behavior. The presented controller decreased RMS common-mode current to 320 mA to 82 mA, which is about a 74% improvement in overall performance compared with the conventional SPWM. This result indicates that many conducted EMI problems in inverter-fed systems can be effectively solved at the source rather than simply treating with external filtering components, since common-mode current is directly responsible for transferring unwanted electromagnetic activity into the line.

A significant observation is made that the EMI reduction was performed without deteriorating power quality. Most traditional mitigation strategies that lead to advancements in EMI performance also come at the expense of higher harmonic distortion or lower output waveform base quality. With the newly proposed framework, Total Harmonic Distortion (THD) was reduced by 4.85% to 2.76% - this proves that EMC objectives and power quality objectives can be optimized at the same time. The potential impact of properly designed EMC-aware control strategies for enhanced electromagnetic compatibility and converter output performance is highlighted by this finding.

The analysis of the models shows that this is standard trade-off behaviour for high performance EMI mitigation techniques. Although good EMI performance was achieved with the proposed controller, a minor loss of converter efficiency was observed. The efficiency reduced from 96.8% at nominal load for a conventional SPWM operation to 95.6% in the case of the EMC-aware controller [9]. This will as a result lower due to more switching constraints bottlenecked by the EMI reduction strategy, and also with respect to the maximization of switching-state transitions. Yet, at over 95 percent efficiency it is still within the acceptable bounds for industrial, renewable energy and transportation applications. Therefore, the results indicate that the performance improvements achievable through EMI reduction far compensates for the limited loss of efficiency.

The compliance evaluation greatly corroborates the proposed method. When operated with conventional SPWM, it gave around -7 dB compliance margin against representative CISPR emission limits. In turn, an implicit margin of +25 dB to the limit value was demonstrated with the proposed framework, implying an enhancement in EMC capability. This is significant because fixing compliance failures usually comes at a cost, as redesigns often involve adding additional filters or shielding structures or adjustments to the grounding structures. The proposed framework integrates EMC consideration into the design and specification process of the controller thereby facilitating compliance-oriented inverter development from day one in initial specifications.

Also, a comparative study of the control strategies examined exposes the pros and cons of current EMI mitigation methods. Results showed that a Random Pulse Width Modulation (PWM) at moderate reduction of harmonics peak emissions, because it can spread harmonic energy on the frequency range. These strategies were further improved with design of optimal switching decisions and eliminating harmonic contents using model

predictive control. Nevertheless, both methods did not attain the EMI suppression effect shown by the explored EMC-aware framework. This observation indicates that conducted EMI reduction mitigation is not a direct result of just control strategy but rather, was an explicit consideration in the required management of EMC objectives.

From the practical side, the benefit of using such a methodology for modern power electronic systems is what follows. Widely, it is implemented in a variety of applications such as EV traction inverter, renewable energy converters, battery energy storage systems industrial motor drives and smart-grid interfaces. Conducted EMI challenges are expected to become increasingly severe as power electronic systems continue to advance toward higher switching frequencies and increased power density. This scalable and future-ready solution is provided by the ability of seamlessly integrate EMC requirements directly into real-time controller design.

Overall, even though promising results were seen in this current study there are important limitations to consider. The validation was conducted in simulation studies first, thus experimental verification is necessary to finalize the effectiveness of the proposed method under practical operating conditions. Second, the study mainly put emphasis on conducted EMI but not radiation one behaviour. Third, in the case study, a three decision unbalance NPC inverter topology was used; further research should analyze adoption of the proposed framework to Flying Capacitor and Cascaded H-Bridge inverter structure. It is also essential to analyze the computational load on future DSP and FPGA implementations established on complex real-time EMI-aware control techniques.

Thus, future studies should emphasize hardware-based confirmation via real-time control systems such as DSPs, FPGAs and Hardware in the Loop (HIL) architectures. Furthermore, other studies might also explore artificial intelligence-assisted EMI prediction frameworks, adaptive EMC-aware smart controllers and digital twin technologies or combined conducted-radiated EMI optimization frameworks. These advances would add even more utility and industrial relevance to EMC-based inverter design processes.

In general, results demonstrate that direct integration of EMC requirements in inverter control design is a great method for conducted EMI reduction with sustained power quality and converter efficiency. An EMC-driven framework for future multilevel inverter systemsThe proposed EMC-driven framework mitigates the limitations of conventional mitigation methods and lays the groundwork for developing next generation high-performance, yet reliable EMC compliant multilevel inverter (MLI) systems.

8. Conclusion and Future Directions

8.1 Conclusion

As number of multilevel inverter technologies have evolved, they are widely used in renewable energy conversion systems and electric vehicles, industrial automation, smart grids Power electronics devices to improve power conversion capability but this increase comes with new EMC challenges. Along with these challenges, conducted EMI (Electromagnetic Interference) is one of the major factors contributing to issues in system reliability, power quality, communication networks and sensitive electronic devices compliance against international regulatory standards. With conventional EMI mitigation approaches mostly passive filters, shielding structures, grounding design and hardware redesign which can lead to greater system cost, weight, complexity & power losses whilst still tackling EMI a posteriori after converter design process is finalized.

This study proposed a new Conducted EMI suppression methodology, an Electromagnetic Compatibility–Driven Design and Real-Time Control Framework for Conducted EMI Reduction in Multilevel Inverters. In contrast to conventional approaches that consider EMC as a post-design compliance requirement, the proposed methodology aims at incorporating electromagnetic compatibility directly into inverter modeling, switching-state selection, modulation strategies and real-time control architectures. The framework reduces emissions but preserves converter efficiency, power quality and dynamic performance by mitigating conducted EMI at its source.

An extensive inverter modeling framework was built in that captures the switching dynamics, common-mode (CM) voltage generation/propagation, CM current propagation, parasitic coupling paths of susceptibility and emissions as well as conducted EMI [3]. On this model, sophisticated EMC-aware control strategies were developed and tested using extensive-simulation studies. A source-level EMI suppression approach was formulated, directly addressing the dominant conduction mechanisms that contribute to electromagnetic emissions.

The proposed framework was shown to be effective from the simulation results. Compared with conventional control strategies, EMI emissions from conducted were remarkably reduced while common-mode voltage and current suppression were significantly advanced. In addition, the proposed controller achieved a good power quality by minimizing total harmonic distortion with respect to other existing techniques and preserving

converter efficiency as far above i.e. industrial level as possible. Results from the compliance assessment indicate high levels of EMC compliance margins with respect to representative CISPR emission limits, demonstrating the promised potential of the proposed strategy enabling standards-compliant inverter design.

These research results validate that EMI conducted via a coupling link can be greatly reduced by smart control while producer also making much less reliance on passive-filter hardware. The proposed framework allows the EMC requirements to be taken into proper consideration by integrating them into inverter operation in a systematic way, as well as offering effective and preventive mechanisms for electromagnetic compatibility (EMC). This will be a major move towards building advanced power electronic systems that possess high efficiency, excellent quality of power, reliable operation and also meet EMC requirements at the same time.

8.2 Research Contributions

The major contributions of this research can be summarized as follows:

1. Development of a comprehensive EMC-driven design methodology for multilevel inverter systems.
2. Investigation and characterization of conducted EMI generation mechanisms, including common-mode voltage, common-mode current, switching harmonics, and parasitic coupling effects.
3. Development of analytical and simulation models capable of representing EMI generation and propagation behavior in multilevel inverter systems.
4. Integration of electromagnetic compatibility requirements directly into real-time inverter control architectures.
5. Design of advanced EMI-aware control strategies capable of reducing conducted emissions at the source.
6. Evaluation of trade-offs between conducted EMI reduction, converter efficiency, harmonic distortion, and dynamic performance.
7. Assessment of compliance with representative EMC standards and conducted emission limits.
8. Establishment of a simulation-based validation framework suitable for future hardware implementation and experimental testing.
9. Provision of practical design guidelines for the development of EMC-compliant inverter systems for industrial and renewable energy applications.

8.3 Future Directions

The proposed framework shows promising results, but there are still many directions for further research and development.

8.3.1 Experimental Hardware Validation

This study is mainly worked around by simulation analysis. The future work is to implement the proposed controller on hardware inverter prototypes and perform experimental measurements with Line Impedance Stabilization Networks (LISNs), spectrum analyzers, current probes and oscilloscopes. While we have proposed a working methodology, experimental validation will give us more confidence about its practical applicability.

8.3.2 Real-Time Implementation on DSP and FPGA

Future research should explore the siting of EMC-aware control algorithms on embedded systems in real time such as:

- Texas Instruments DSP controllers
- Xilinx FPGA platforms
- Zynq System-on-Chip devices
- Industrial real-time controllers

These implementations would allow for evaluation of controller execution time, computational complexity, resource usage, and deployment limits.

8.3.3 Hardware-in-the-Loop (HIL) Validation

Analogue Hardware-in-the-Loop environments like OPAL-RT, Typhoon HIL, and dSPACE platforms can be useful to test this proposed framework in a realistic environment before moving into the actual hardware level. HIL testing would allow for fast prototyping and evaluation of controllers.

8.3.4 Artificial Intelligence-Based EMI Prediction

The potential of electromagnetic interference (EMI) prediction and adaptive control technologies are wide open in the context of machine learning and artificial intelligence techniques. Future studies may investigate:

- Neural network-based EMI prediction models
- Reinforcement learning control strategies

- Adaptive switching optimization algorithms
- Data-driven EMC monitoring systems

These approaches could enhance controller adaptability and improve real-time EMI suppression performance.

8.3.5 Digital Twin-Based EMC Monitoring

Digital twin technologies are beginning to be a really useful technology for real-time monitoring and prediction in power electronic systems. The use of digital twins for future EMC-aware inverter systems might be:

EMI behavior prediction in real time

Identify compliance violations before they happen

Optimize controller parameters dynamically

Support predictive maintenance strategies

8.3.6 Wide-Bandgap Semiconductor Applications

Investigating the Proposed Framework: Future research should leverage our proposed framework applied to inverter systems using emerging semiconductor technologies, such as:

- Silicon Carbide (SiC) MOSFETs
- Gallium Nitride (GaN) transistors
- These devices enable better efficiency and switching performance while contributing to higher EMI challenges with extremely high dv/dt and di/dt switching characteristics.

8.3.7 Radiated EMI Integration

This work has primarily focused on conducted emissions. Further work will be to enhance a full EMC-oriented inverter design methodology by including the analysis and suppression of radiated EMI. Such work may include:

- Electromagnetic field modeling
- Shielding optimization
- PCB layout optimization
- Cable routing analysis

8.3.8 Adaptive EMC-Aware Controllers

Next-generation inverter systems could utilize adaptive control architectures that can dynamically alter switching patterns and control parameters based on real-time EMI measurements and operating conditions. These controllers might automate and periodically optimize EMC performance.

8.3.9 Multiobjective Optimization and Reliability Assessment

Future studies may apply the optimization framework to the relationship between additional objectives, such as:

- Thermal performance
- Reliability prediction
- Device lifetime estimation
- Fault tolerance
- Energy efficiency

This would allow to optimize the electromagnetic compatibility and long-term system reliability simultaneously.

8.3.10 Application to Emerging Energy systems

The methodology outlined in this paper is extensible and can be further applied for future use cases, including:

- Electric vehicle traction systems
- Fast EV charging infrastructure
- Renewable energy converters
- Smart-grid interfaces
- Aerospace power electronics
- Marine electrification systems
- Battery energy storage systems

Such application domains will enforce more and more stringent EMC requirements opening the design methodologies driven by EMC at the bottom of the pyramid for future developments.

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